WPM 4.4: An 18b 20KHz Dual ΣΔ A/D Converter

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Sigma-delta noise shaping has been used in A/D converters to increase dynamic range without increasing the accuracy demands placed on individual components. Stable, single-bit higher-order loops have been designed that extend the dynamic range of ΣΔ converters while retaining low component accuracy requirements.[1,2] This paper describes a dual, 20kHz bandwidth, 18b ΣΔ ADC with an oversampling ratio of 64 and a noise floor that is 105dB below full scale. The converter is implemented on two chips: a 10V 3μm CMOS modulator chip, and a 5V 1.5μm CMOS decimator chip.

A block diagram of the circuit is shown in Figure 1. The modulator chip contains a dual-output 3.0V reference, clocking and interface circuitry, and two fifth-order one-bit fully-differential switched-capacitor ΣΔ modulators. Each modulator contains five amplifiers, a comparator, switches, capacitors and associated non-linear stabilization circuitry. The decimator chip has been described previously.[3] The switched-capacitor architecture for the ΣΔ modulators was designed following a procedure described in a previous publication.[2] Figure 2 is a single-channel single-ended representation of the switched-capacitor architecture used. A fully-differential architecture is used to increase signal swing and power supply rejection while reducing the effects of substrate coupling and digital feedthrough. This architecture has a more elaborate reference switching scheme than in the single-ended representation, with one stage of it represented in Figure 3. The signals "X" and "XBar" are the true and complement outputs of the comparator. The differential architecture is fully-pipelined, and notches in the quantization error transfer function are implemented using switched-capacitor resonators, also described previously.[2] The capacitors are sized from kTC noise considerations and the switches sized to allow 18b settling of the charge transfer in one-half clock period, or 160ns.

Figure 4 shows the simulated and measured signal and quantization error transfer functions of the switched-capacitor filter with the comparator removed. The clock is slowed down in order to accommodate the external circuitry needed to make the measurement.

Higher-order modulators are stable over a limited range of "1's" density at the output and over a limited range of integrator states.[1,2] Instability in this modulator is sensed digitally, by counting the number of consecutive ones or zeros in the modulator bit stream. A sufficiently long string of either "1's" or "0's" indicates modulator instability and triggers circuitry which resets the state in the integrators to put the modulator into a stable operating condition.

A single 3.0V bandgap reference with separate left and right output stages is included in the part, with a reference voltage fed back to each channel independently using a switched-capacitor single-ended to differential converter and a selector controlled by the comparator, as represented in Figure 3. The bandgap reference takes advantage of parasitic bipolar devices available in a standard CMOS process. These devices are stacked to reduce the effects of MOS threshold mismatches on the output voltage and temperature drift performance.

The performance of the input amplifier in higher-order loops determines overall converter performance. To achieve the stated performance, the following features were designed into the front-end amplifier: (1) fully differential, including a common mode loop. (2) settling to 18b accuracy (23μV) in one-half clock cycle (120ns). (3) gain linearity of 0.001%, or 10μV peak non-linearity over the entire 3V peak output range. (4) chopper stabilization (between the clock phases) to eliminate offset and 1/f noise contributions. (5) input-referred thermal noise contribution below the modulator noise floor of -105dB full scale.

A simplified circuit diagram of the amplifier is shown in Figure 5. A single-stage folded-cascode architecture is chosen for both the differential and common-mode paths. This topology has an inherently high bandwidth, which enables the amplifier to meet settling time specifications. A mirror is not used in the common-mode signal path to make the bandwidth of this path equal to that of the differential signal path. Compensation for both the common-mode and differential-mode paths is provided using the switched-capacitor circuit capacitances surrounding the amplifier.

The common-mode output voltage is sensed using pMOS source followers on each output driving a resistive and capacitive summing network at the output. The summed voltage is compared to ground through an nMOS differential pair, and the difference current is fed back to the amplifier to control the common-mode current.

The amplifier linearity is limited by impact ionization current in the nMOS output devices. This current causes an effective non-linear resistive load on the amplifier, and therefore a gain non-linearity. The problem is corrected by placing an nMOS transistor between the output and the nMOS current source and driving its gate so that a low drain-source voltage is maintained across all nMOS signal transistors, reducing their impact ionization current dramatically. The correction circuitry improves the third harmonic distortion of the amplifier from -88dB to -106dB.

Table 1 shows the measured performance of the converter. Figure 6 is a plot of signal/(THD+noise) versus signal for the converter. Figure 7 is a package photograph showing both the modulator and decimator chips.

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References

[1]Lee, W. L. and C.G. Sodini, "A Topology for Higher-Order Interpolative Coders", ISCAS Proc. 1987

[2]Ferguson, P. F. et al., "One Bit Higher Order Sigma-Delta A/D Converters", ISCAS PROC. 1990, vol. 2, pp. 890-893,

[3]Dattorro, J. et al., "The Implementation of One-Stage Multirate 64:1 FIR Decimator for use in One-Bit Sigma-Delta A/D Applications", AES 7th International Conference, May 1989

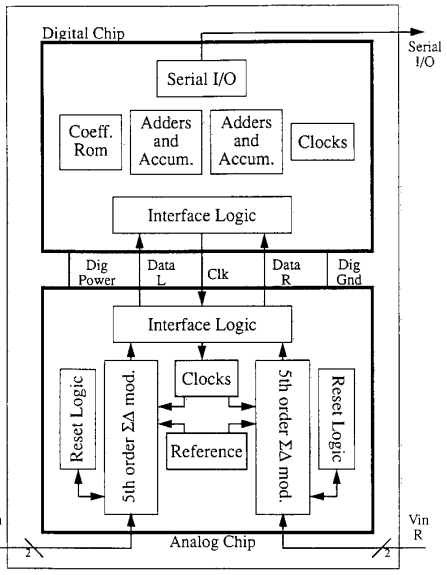
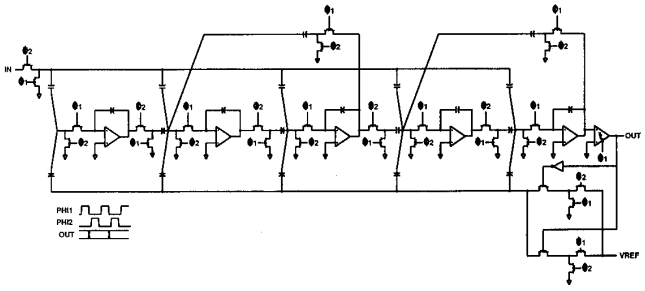


Figure 1: Block diagram of ADC (left)

Figure 2: Single-channel single-ended representation of the architecture (below)



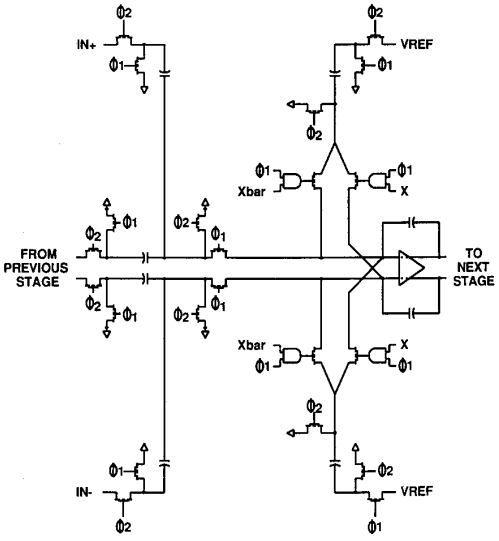


Figure 3: Representation of one stage of the differential architecture

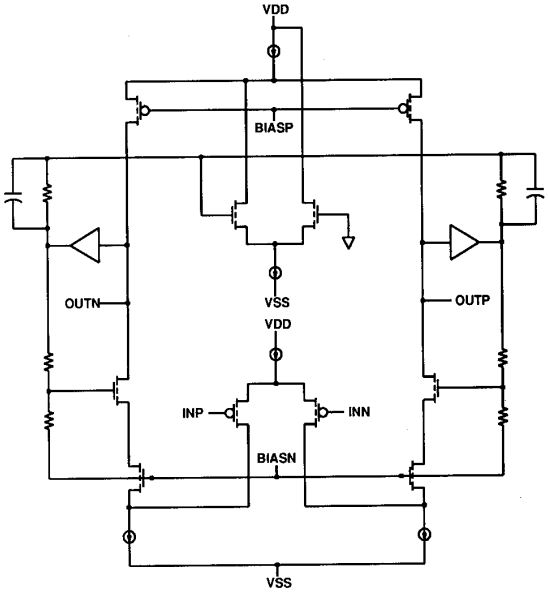


Figure 5: Simplified circuit diagram of the sampler

FIGURE 4 – *See page 292*

FIGURE 7 – *See page 292*

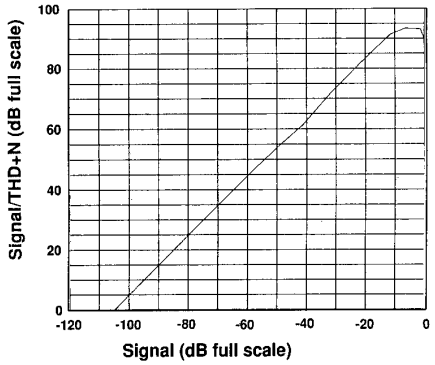


Figure 6: Signal/(THD+noise) vs. signal for the converter

Interchannel crosstalk	-110dB at 1kHz
Converter noise floor	-105dBFS
Input range	±6V (differential)
Signal bandwidth	20kHz
Decimator passband ripple	0.001dB
Decimator stopband atten.	115dB
Modulator die size	6.8x4.7mm
Decimator die size	6.8x5.5mm
Power dissipation	900mW
Package	28-pin 600mil plastic DIP

Table 1: Measured converter performance

(Continued from page 69)

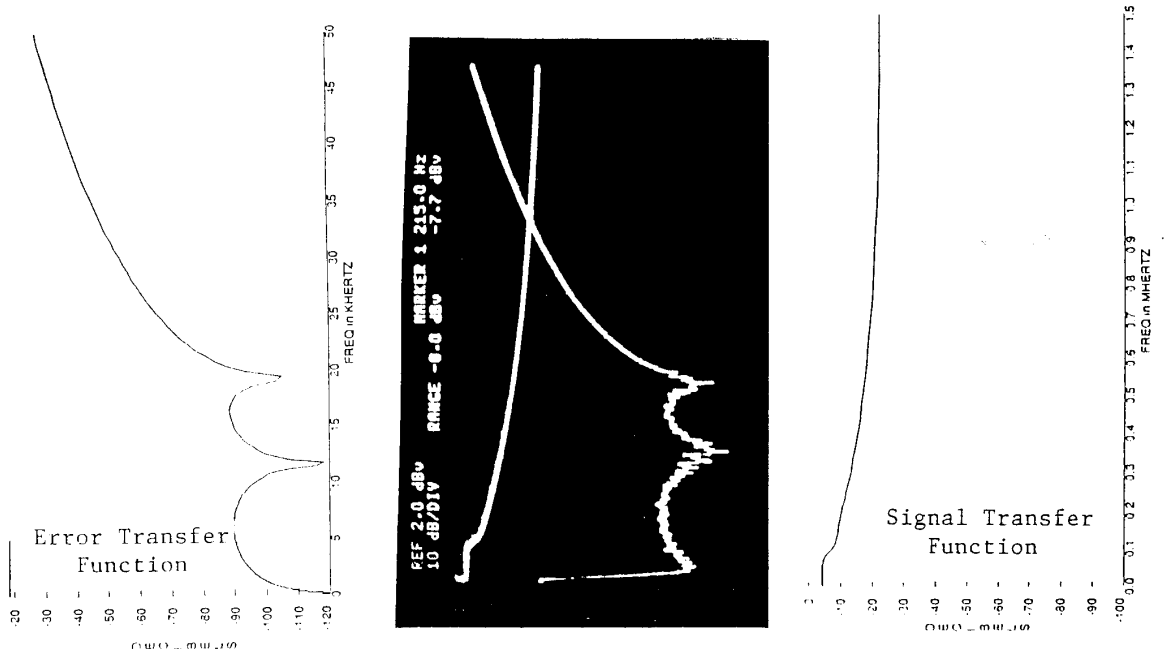


Figure 4: Simulated and measured signal and quantization error transfer functions

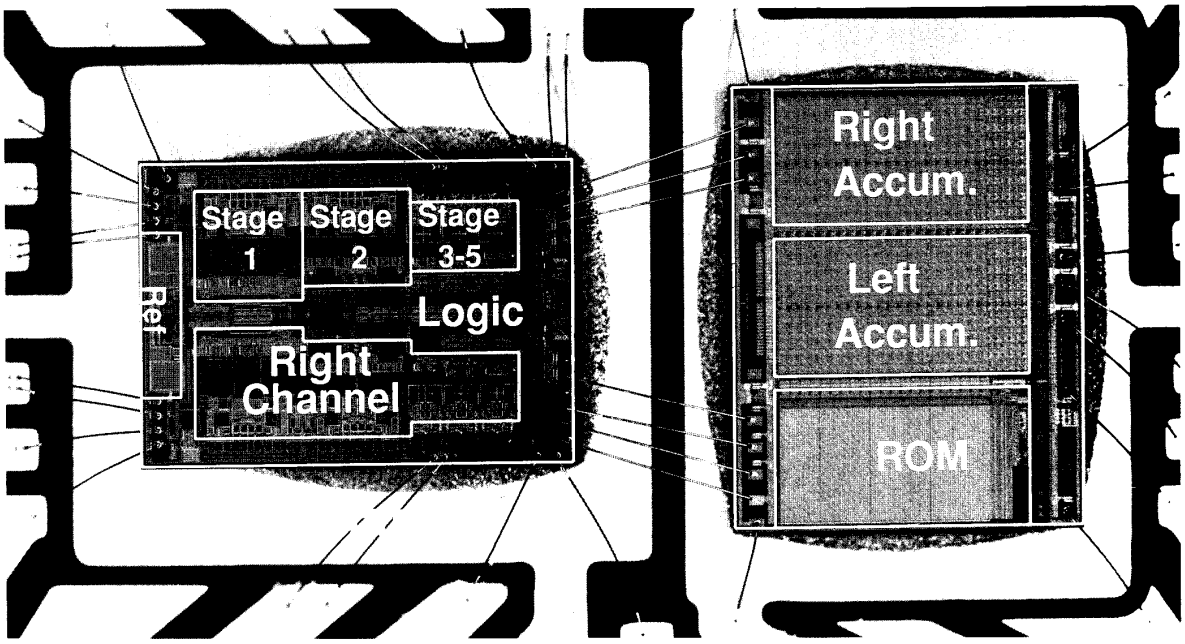


Figure 7: Package photograph of the 18b stereo ADC