Vol 53 No 4, October 2019

ANALOG DEVICES
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AnalogDialogue

A Direct Method of Measuring Op Amp Input Differential Capacitance

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Introduction

Input capacitance can be a key specification for high impedance and high frequency operational amplifier (op amp) applications. Notably, when photodiode junction capacitance is small, the op amp input capacitance can dominate noise and bandwidth issues. The op amp input capacitance and the feedback resistor create a pole in the amplifier's response, impacting stability and increasing the noise gain at higher frequencies. As a result, stability and phase margin could degrade and output noise could increase. In fact, some previous C_{DM} (capacitance—difference mode) measurement techniques were based on high impedance inverting circuits and stability analysis, as well as noise analysis. These techniques can be quite tedious.

In a feedback amplifier such as an op amp, total effective input capacitance is comprised of C_{DM} in parallel with the negative input common-mode capacitance, or C_{CM-}, to ground. One of the reasons C_{DM} is difficult to measure is that the op amp's main task is keeping the two inputs from separating. Compared to the difficulty of C_{DM} measurement, measuring positive input common-mode capacitance, C_{CM+}, to ground directly is relatively easy. By putting a large series resistance in the noninverting pin of the op amp and applying a sine wave or noise source, the –3 dB frequency response due to the op amp input capacitance is measured using a network analyzer or a spectrum analyzer. C_{CM+} and C_{CM-} are assumed to be identical, especially for voltage feedback amplifiers. However, measuring C_{DM} has been more elusive through the years; various techniques used were dissatisfying due to the inherent nature of an op amp to force its inputs to be equal, bootstrapping the C_{DM}. When the inputs are forced apart and current is measured, the output tries to counter. Traditional methods of probing C_{DM} are indirect, relying on phase margin degradation and being complicated by other capacitances such as C_{CM-} in parallel.

It is desired that the op amp under test be truly operational and functioning, as it normally would be under closed-loop conditions, just as customers use them. One possibility suggested was to split the inputs and let the output clip, but depending on the op amp topology, this could render internal circuitry nonoperational, so the measured capacitance may not reflect actual operational capacitance. In this approach, the inputs are not split too much to avoid nonlinearities in the input stage as well as excessive output swing or clipping. This article will present a simple and direct method of measuring C_{DM}.

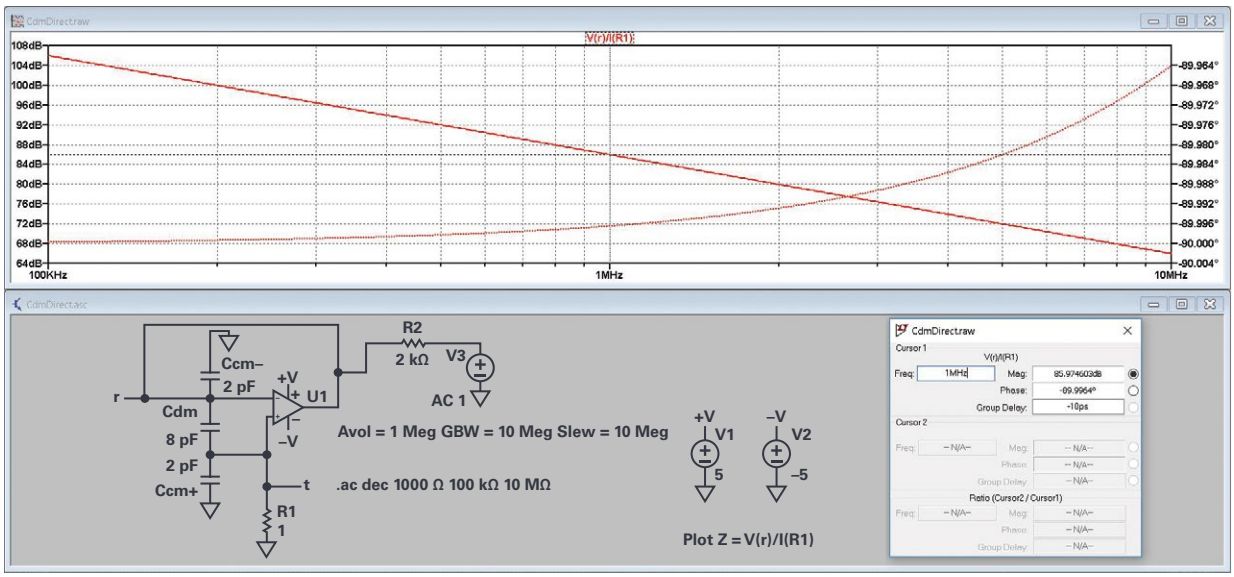

Figure 1. Direct measurement of C_{DM} impedance in LTspice. Plot V(r)/I(R1) to get the impedance. In this case, at 1 MHz, Z is 19.89437 kΩ ($10^{85.97/20}$) at –89.996°, which is exactly 8 pF using C = 1/(2π × Z × Freq).

A New Way to Measure C_{DM}

The authors decided to simply use a gain of 1 buffer circuit and excite the output and inverting input with a current source. The output and inverting input will move only as much as the op amp allows. At low frequencies, the output will move very little, so the current through C_{DM} would be small. And at too high frequencies, the test may not be valid, nor the results useful. But at medium frequencies, where the gain-bandwidth of the op amp is falling but still not too low, the output motion could be adequate to provide enough voltage excitation and a measurable current through C_{DM}.

The practically unlimited noise floor of LTspice® enabled a simple test simulation, shown in Figure 1. After seeing the technique work rather exactly in LTspice, the question became "will I have adequate SNR in the real world to make a good measurement?"

The angle is almost equal to –90°, which indicates that the impedance is capacitive. The 2 pF common-mode capacitances did not corrupt the measurement because C_{CM-} is not in the path and $1/(2 \times \pi \times Freq \times C_{CM+}) >> 1\ \Omega$.

Challenges: Finding the Right Equipment and Actual Test Setup

Looking at Figure 1, the 2 kΩ is put in series at the op amp output to transform the excitation from a voltage source to a current source. This will allow a small voltage in node "r," which should be not too far from the voltage that will be seen in the noninverting pin of the op amp and will cause small current to flow in between the inputs for the C_{DM} to be measured. Now, of course, the output voltage is small, being buffered by the device under test (DUT), and also the current in C_{DM} is very small (57 nA in the sim), so measuring it using a 1 Ω resistor would be difficult on the bench. LTspice.ac and LTspice.tran simulations do not have resistor noise, but a 1 Ω resistor in the real world has 130 pA/√Hz and would render only 57 nV of signal from our anticipated 57 nA of capacitor current. Further simulations showed that replacing R1 with 50 Ω or 1 kΩ would not result in too much lost current into C_{CM+} at frequencies within the bandwidth of interest. For a better current measurement technique than a simple resistor, a transimpedance amplifier (TIA) could be used instead to replace R1. The TIA input would be connected to the noninverting pin of the op amp where the current is desired while fixing the voltage at virtual ground to preclude current in C_{CM-}. It turns out that this is exactly how four-port impedance analyzers such as the Keysight/Agilent HP4192A are implemented. The HP4192A can measure impedance over frequencies from 5 Hz to 13 MHz. Some of the newer pieces of equipment in the market that use the same impedance measurement technique are the E4990A impedance analyzer with 10 Hz to 120 MHz range and precision LCR meters like Keysight E4980A with 20 Hz to 2 MHz range.

Looking at the test circuit in Figure 2 below, the noninverting pin of the op amp is in virtual ground due to the TIA inside the impedance analyzer. Because of this, C_{CM+} would not affect the measurement since both of its terminals will be seen to be at ground potential. The small current developed across the C_{DM} of the DUT will flow through the feedback resistor R_r of the TIA, which is then measured with the internal voltage meter.

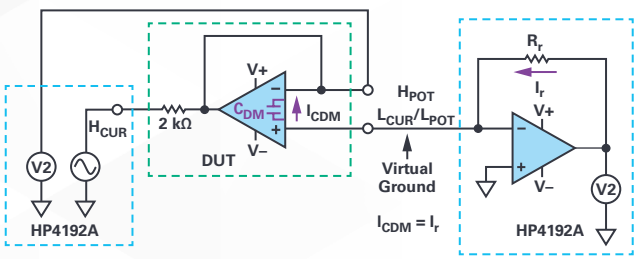

Figure 2. Test circuit for C_{DM}.

Any four-port equipment that uses the autobalancing bridge[1] impedance measurement method can be a good candidate to measure C_{DM}. They are designed to generate a sine wave from an internal oscillator which is centered at zero with positive and negative swings for dual supply operation. If the op amp DUT is being powered in single supply, the bias function should be adjusted, so that the signal is not clipped against ground. In Figure 3, an HP4192A was used with the detailed connections going to the DUT.

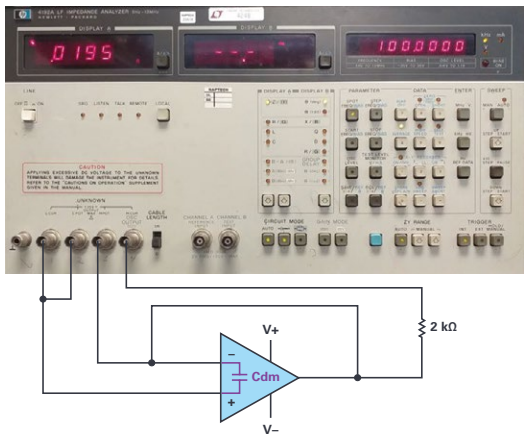

Figure 3. Direct C_{DM} measurement method test setup.

Figure 4 shows the exact test setup used to achieve a very minimal parasitic capacitance contribution to C_{DM} from the board and wiring. Any general-purpose board can be used for slow op amps while high speed op amps demand stricter PCB board layout. The vertical grounded copper board dividers are placed to make sure to prevent the input and output from seeing additional field paths in parallel with the DUT C_{DM}.

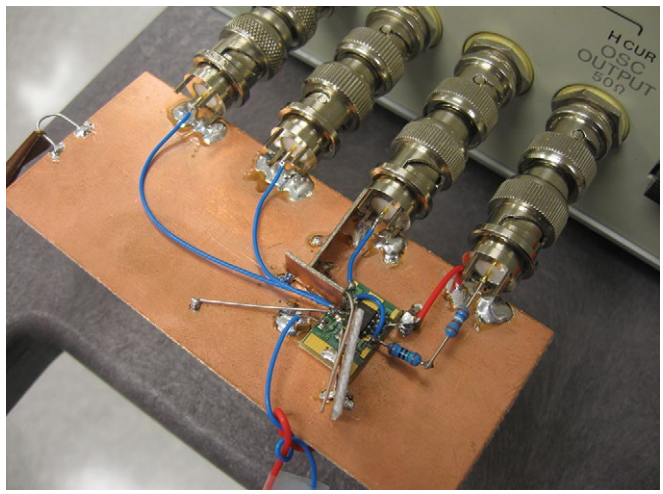

Figure 4. The HP4192A setup showing the board. Excitation through 2 kΩ and voltage readback are on the right. The DUT used is an LT1792 8-lead SO on a single postage stamp LB2223. TIA is on the left, internal to HP4192A.

Results and Discussions

First, the board is tested without the DUT to measure its board capacitance. The board shown in Figure 4 was measured at 16 fF of DUT-less capacitance. This is a relatively small capacitance that can be neglected, as C_{DM} values are typically expected in hundreds to thousands of femtofarads.

Most JFET and CMOS input op amps were measurable using this new C_{DM} measurement technique. As an example, to illustrate the method, an LT1792 low noise precision JFET op amp was measured. The table below lists the impedance (Z), phase angle (θ), reactance X_S, and the calculated C_{DM} across a range of frequencies. Impedance exhibits a purely capacitive nature when the phase angle is –90°.

Table 1. LT1792 Impedance Measurement Across Frequencies at ±15 V Supply

Frequency	Z (kΩ)	θ	X_S (kΩ)	$C_S = C_{DM} = 1/(2 \times \pi \times X_S \times Freq)$ (pF)
500 kHz	33	–89°	–32.9	9.7
600 kHz	27	–90°	–26.9	9.8
700 kHz	22.6	–90°	–22.6	10
800 kHz	19.65	–90°	–19.7	10.1
900 kHz	17.4	–90°	–17.4	10.2
1 MHz	15.64	–89.9°	–15.6	10.2
2 MHz	7.76	–89.8°	–7.76	10.25
3 MHz	5.1	–90°	–5.1	10.4
4 MHz	3.74	–90°	–3.74	10.6
5 MHz	2.92	–90°	–2.92	10.9

Table 1 above gives results measured in the frequency range of 500 kHz to 5 MHz. The phase in this frequency range is close to being purely capacitive with a phase of –89° to –90°. Also, the reactance X_S dominates the total input impedance such that $Z \approx X_S$. The averaged computed C_{DM} is around 10.2 pF. Maximum frequency of measurement is 5 MHz because this part bandwidth is up to 5.6 MHz only. Results at lower frequencies became incoherent. This was presumably due to a quickly vanishing C_{DM} current, with output voltage reduced by op amp action, while X_S also becomes a higher impedance at low frequency.

The output of the op amp should also be checked at each step frequency to make sure that it is not being overdriven by the signal coming out from the impedance analyzer. The amplitude of this signal from HP4192A can be adjusted from 0.1 V to 1.1 V, just enough to create a wiggle in the output of the op amp and move the voltage level a little in the inverting input pin. Figure 5 shows a 28 mV peak-to-peak undistorted signal (green signal) at the output of the op amp at frequency equals 800 kHz. The yellow signal with 2.76 V peak-to-peak amplitude (1 V rms) is probed directly from the oscillating output port of the analyzer. It is arbitrarily decided not to allow distortion in the output, out of fairness, both to the DUT and to the HP4192A detectors. The probes were removed when getting the actual data of impedance and phase, although the setup is relatively immune to their effects.

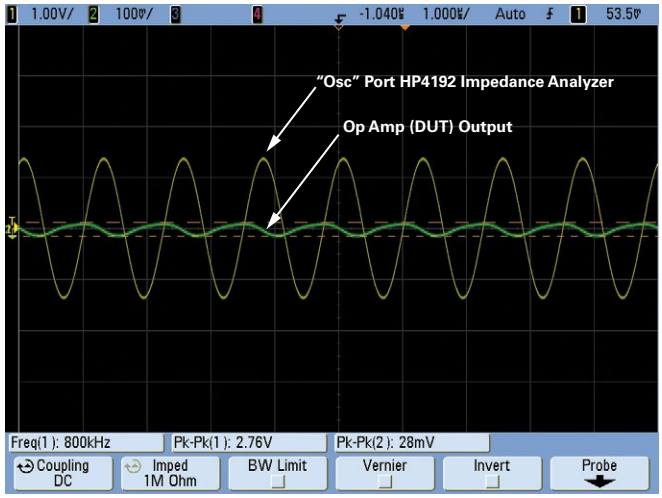

Figure 5. Probed outputs of HP4192A "Osc" output port and op amp output pin.

A test was also done to measure C_{DM} on a different supply voltage. The dependence of C_{DM} on supplies and common-mode voltage may vary across different op amps; different topologies and transistor types are expected to result in different junction parasitics to high and low supplies. Table 2 shows the results for the ±5 V supply still with the LT1792. The average measured C_{DM} is 9.2 pF, which is relatively close to the result of 10 pF with ±15 V supply. Thus, it could be concluded that LT1792 C_{DM} does not change significantly by changing the supply voltage. This is in stark contrast to its C_{CM}, which varies considerably with supply voltage.

Table 2. LT1792 Impedance Measurement Across Frequencies at ±5 V Supply

Frequency	Z (kΩ)	θ	X_S (kΩ)	$C_S = C_{DM}$ (pF)
500 kHz	37	–90°	–37	8.6
600 kHz	30	–91°	–30	8.8
700 kHz	25.3	–91°	–25.2	9
800 kHz	22	–91°	–22	9
900 kHz	19.5	–91°	–19.5	9
1 MHz	17.5	–91°	–17.5	9.1
2 MHz	8.62	–92°	–8.62	9.2
3 MHz	5.6	–93°	–5.6	9.5
4 MHz	4.07	–94°	–4.07	9.8
5 MHz	3.14	–94°	–3.14	10.1

Meanwhile, bipolar input op amps are almost as straightforward compared to their FET counterparts. However, their high input bias current and current noise will be noticed, as these are in parallel with the C_{DM} current. Added to that is the intrinsic differential resistance R_{DM} inherent in bipolar differential pair inputs, also in parallel with C_{DM}. Using ADA4004, a low noise precision amplifier as a sample, Table 3 shows the impedance measurements. Obviously, the phase does not indicate a purely capacitive behavior, as it is far from –90°. Although, the 4 MHz, 5 MHz, and 10 MHz frequencies are quite close, a parallel equivalent impedance RC model would fit this case, to be able to extract the C_{DM} out of the other resistances. Therefore, parallel conductance G_P, susceptance B_P, and the calculated C_{DM} across a range of frequencies are shown in Table 3, wherein C_P is assumed to be equal to C_{DM}.

Table 3. ADA4004 Impedance Measurement Across Frequencies at ±15 V Supply

Frequency	Z (kΩ)	θ	G_P (µS)	B_P (µS)	$C_P = C_{DM} = B_P/(2 \times \pi \times Freq)$ (pF)
500 kHz	29.4	–36°	27.5	20	6.4
600 kHz	27.2	–41°	27.6	24.1	6.4
700 kHz	25.3	–45.4°	27.6	28	6.4
800 kHz	23.5	–49°	27.9	32	6.4
900 kHz	22	–52°	28	35.7	6.3
1 MHz	20.7	–54.3°	28.1	39.3	6.3
2 MHz	12	–72.6°	24.9	79.4	6.3
3 MHz	7.8	–79.2°	24	126	6.7
4 MHz	5.8	–81.8°	24.5	171	6.8
5 MHz	4.7	–83.5°	24.2	212.7	6.8
10 MHz	2.5	–86°	28	319.5	6.3

Based on the results in Table 3, ADA4004 C_{DM} can be estimated to be around 6.4 pF. The results also imply that across the frequency range presented in Table 3, C_{DM} has some substantial parallel conductance G_P and is not a purely capacitive C_{DM}. The measurement is revealing the approximate 40 kΩ (25 µS) of real input differential resistance in this bipolar op amp.

Additional note: Attempts were made at measuring other types of op amps such as zero-drift op amps (LTC2050) and high speed bipolar op amps (LT6200). Results were incoherent, presumably because of switching artifacts in the zero-drift op amp and excessive current noise in the high speed bipolar op amp.

Conclusion

C_{DM} is not a difficult measurement. One caveat is that the HP4192A reports an impedance in magnitude and angle. The capacitance reading assumes a simple series of RCs or parallel RCs, whereas op amp input impedance can be much more complicated. The capacitance reading should not necessarily just be taken at face value. Each op amp is also a unique case of its own. The frequency range wherein a capacitive reactance dominates the input impedance may vary from design to design. The input stage design, devices and processes used, Miller effects, and packaging could all contribute to the totality of the differential input impedance and its measurement. A JFET input op amp and a bipolar input op amp were measured, revealing both C_{DM} and in the case of the bipolar input op amp, R_{DM} results.

References

[1] Gustaaf Sutorius. "Challenges and Solutions for Impedance Measurements." Keysight Technologies, March 2014.

Acknowledgements

Glen Brisebois would like to thank Brian Hamilton for this challenge, Aaron Schultz and Paul Henneuse for their support, and Henry Surtihadi, Kaung Win, Barry Harvey, and Raj Ramchandani for their input.

Arthur Roxas would like to thank Paul Blanchard, Matt Duff, Jess Espiritu, and Kristina Fortunado for the opportunity to work on this project with Glen.

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